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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,059	04/08/2002	Christopher James Lloyd	39-253	7188

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EXAMINER	
FOX, JAMAL A	
ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,059	LLOYD, CHRISTOPHER JAMES	
	Examiner	Art Unit	
	Jamal A. Fox	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,11-13,15 and 19-22* is/are rejected.

7)☒ Claim(s) *6,10,14 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C, § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/030,059.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/8/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 22 provides for the use of signal processing, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim 22 is rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd.* v. *Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

4. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: A common multiplexer, input channels, output circuit, predetermined repeating sequence, predetermined signal, AND gate, NOT gate, and a marker channel. These elements

are essential because they allow a large number of signals to be monitored in parallel using relatively simple electronics.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3-5, 7-9, 11-13, 15, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Smither et al. (U.S. Patent No. 3,959,767).

Referring to claim 1, Smither et al. discloses a signal processing apparatus (Fig. 1 and respective portions of the spec.) comprising a plurality of input channels (Fig. 1 ref. sign 16 and respective portions of the spec.) each of which is connected to a respective input of a multiplexer (Fig. 1 ref. sign 18 and respective portions of the spec.), the multiplexer being arranged to connect each input to a common multiplexer output (Fig. 1 ref. sign 26 and respective portions of the spec.) in a predetermined repeating sequence (sequence, col. 3 lines 55-60), and an output circuit (Fig. 1 ref. sign 30 and respective portions of the spec.) connected to the common multiplexer output, wherein the output circuit is arranged to detect the presence at the common multiplexer output of a predetermined signal (signal, col. 3 lines 19-63), to identify the input channel which was the source of the detected predetermined signal, and to output (output, col. 3 lines 45-50) a signal representative of the identified input channel.

Referring to claim 3, Smither et al. discloses a signal processing apparatus (Fig. 1 and respective portions of the spec.) according to claim 1, wherein each input channel (Fig. 1 ref. sign 16 and respective portions of the spec.) is connected to the multiplexer (Fig. 1 ref. sign 18 and respective portions of the spec.) for a time sufficient to determine whether the predetermined signal (signal, col. 3 lines 19-63) is present at the input, but is not connected for a time sufficient to allow a signal representative of that input channel to be output unless the predetermined signal (signal, col. 3 lines 19-63) is detected.

Referring to claim 4, Smither et al. discloses a signal processing apparatus according to claim 3, wherein, if the predetermined signal (signal, col. 3 lines 19-63) is detected, the input channel (Fig. 1 ref. sign 16 and respective portions of the spec.) is connected to the multiplexer (Fig. 1 ref. sign 18 and respective portions of the spec.) input for a time sufficient to transfer the signal (signal, col. 3 lines 19-63) representative of that input channel to a data latch (Fig. 2 ref. sign 118 and respective portions of the spec.).

Referring to claim 5, Smither et al. discloses a signal processing apparatus according to claim 4, wherein the data latch is connected to a storage means (memory, col. 6 lines 60-65).

Referring to claim 7, Smither et al. discloses a signal processing apparatus according to claim 1, wherein the multiplexer is controlled by a counter (counter, col. 6 lines 21-52), and the signal representative of the identified input channel comprises the number generated by the counter (counter, col. 6 lines 21-52).

Referring to claim 8, Smither et al. discloses a signal processing apparatus according to claim 7, wherein the counter is driven by a clock (Fig. 2 ref. sign 86 and respective portions of the spec.).

Referring to claim 9, Smither et al. discloses a signal processing apparatus according to claim 7, wherein the counter is a self-rollover counter arranged to recommence (reset, col. 6 lines 45-52) the sequence after a final input channel of the predetermined sequence has been connected to the common multiplexer output.

Referring to claim 11, Smither et al. discloses a signal processing apparatus according to claim 1, wherein at least some of the input channels are connected to detectors (Fig. 3 ref. sign 64 and Fig. 2 ref. sign 92 and respective portions of the spec.).

Referring to claim 12, Smither et al. discloses a signal processing apparatus according to claim 11, wherein at least one detector includes means (counter, col. 6 lines 21-52) to accumulate a signal representative of events incident at that detector.

Referring to claim 13, Smither et al. discloses a signal processing apparatus according to claim 11, wherein at least one detector is provided with detector reset (reset, col. 6 lines 40-52) means arranged to reset that detector once the signal representative of the input channel has been transferred to a data latch.

Referring to claim 15, Smither et al. discloses a signal processing apparatus according to claim 5 or any claim dependent thereon, further comprising data conversion means (Fig. 1 ref. sign 32 and respective portions of the spec.) for converting signals stored in the storage means into a series of sets of data, each set of

data being representative of the incidence of the predetermined signal at a particular input channel.

Referring to claim 19, Smither et al. discloses a method of signal processing comprising connecting each of a plurality of input channels (Fig. 1 ref. sign 16 and respective portions of the spec.) in a predetermined repeating sequence (sequence, col. 3 lines 55-60) to a common multiplexer output (Fig. 1 ref. sign 26 and respective portions of the spec.) via respective multiplexer inputs, and connecting the common multiplexer output to an output circuit (Fig. 1 ref. sign 30 and respective portions of the spec.), wherein the method further comprises detecting the presence at the common multiplexer output of a predetermined signal (signal, col. 3 lines 19-63), identifying the input channel which was the source of the detected predetermined signal (signal, col. 3 lines 19-63), and outputting (output, col. 3 lines 45-50) a signal representative of the identified input channel.

Referring to claim 20, Smither et al. discloses a method of signal processing according to claim 19, and incorporating the apparatus (Fig. 1 and respective portions of the spec.).

7. Claims 1, 3, 4, 7 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Rittenberry et al. (U.S. Patent No. 4,704,609).

Referring to claim 1, Rittenberry et al. discloses a signal processing apparatus (Drawing Figure and respective portions of the spec.) comprising a plurality of input channels (Figure ref. signs 8, 10 and 12 and respective portions of the spec.) each of which is connected to a respective input of a multiplexer (Figure ref. sign 4 and

respective portions of the spec.), the multiplexer being arranged to connect each input to a common multiplexer output (Figure ref. sign 6 and respective portions of the spec.) in a predetermined repeating sequence (sequence, col. 1 lines 65-68 and col. 6 lines 15-20), and an output circuit (Figure ref. signs 28, 30, 32, 42, 44, 46, 48, 50 and 52 and respective portions of the spec.) connected to the common multiplexer output, wherein the output circuit is arranged to detect the presence at the common multiplexer output of a predetermined signal (signal, col. 3 lines 40-45), to identify the input channel which was the source of the detected predetermined signal (signal, col. 3 lines 40-45), and to output (applied, col. 3 lines 40-45) a signal representative of the identified input channel.

Referring to claim 3, Rittenberry et al. discloses a signal processing apparatus (Drawing Figure and respective portions of the spec.) according to claim 1, wherein each input channel (Figure ref. signs 8, 10 and 12 and respective portions of the spec.) is connected to the multiplexer (Figure ref. sign 4 and respective portions of the spec.) for a time sufficient to determine whether the predetermined signal (signal, col. 3 lines 40-45) is present at the input, but is not connected for a time sufficient to allow a signal representative of that input channel to be output unless the predetermined signal (signal, col. 3 lines 40-45) is detected.

Referring to claim 4, Rittenberry et al. discloses a signal processing apparatus (Drawing Figure and respective portions of the spec.) according to claim 3, wherein, if the predetermined signal (signal, col. 3 lines 40-45) is detected, the input channel (Figure ref. signs 8, 10 and 12 and respective portions of the spec.) is connected to the multiplexer (Figure ref. sign 4 and respective portions of the spec.) input for a time

sufficient to transfer the signal (signal, col. 3 lines 40-45) representative of that input channel to a data latch (Figure ref. sign 74 and respective portions of the spec.).

Referring to claim 7, Rittenberry et al. discloses a signal processing apparatus according to claim 1, wherein the multiplexer is controlled by a counter (Figure ref. sign 20 and respective portions of the spec.), and the signal representative of the identified input channel comprises the number generated by the counter (Figure ref. sign 20 and respective portions of the spec.).

Referring to claim 19, Rittenberry et al. discloses a method of signal processing comprising connecting each of a plurality of input channels (Figure ref. signs 8, 10 and 12 and respective portions of the spec.) in a predetermined repeating sequence (sequence, col. 1 lines 65-68 and col. 6 lines 15-20) to a common multiplexer output (Figure ref. sign 6 and respective portions of the spec.) via respective multiplexer inputs, and connecting the common multiplexer output to an output circuit (Figure ref. signs 28, 30, 32, 42, 44, 46, 48, 50 and 52 and respective portions of the spec.), wherein the method further comprises detecting the presence at the common multiplexer output of a predetermined signal (signal, col. 3 lines 40-45), identifying the input channel which was the source of the detected predetermined signal (signal, col. 3 lines 40-45), and outputting (applied, col. 3 lines 40-45) a signal representative of the identified input channel.

8. Claims 1 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Abe (EP 0 350 932 A2).

Referring to claim 1, Abe discloses a signal processing apparatus (Fig. 2 and respective portions of the spec.) comprising a plurality of input channels (Fig. 2 ref. signs 47-54 and respective portions of the spec.) each of which is connected to a respective input of a multiplexer, the multiplexer being arranged to connect each input to a common multiplexer output (Fig. 2, see the arrow going from the multiplexer to the A/D Converting Unit) in a predetermined repeating (repeat, col. 4 lines 50-58, col. 5 lines 35-40 and col. 8 lines 35-40) sequence, and an output circuit (Fig. 2 ref. sign 45 and respective portions of the spec.) connected to the common multiplexer output, wherein the output circuit is arranged to detect (Fig. 2 ref. sign 46 and respective portions of the spec.) the presence at the common multiplexer output of a predetermined signal (signal, col. 7 line 25 – col. 8 line 20), to identify the input channel which was the source of the detected predetermined signal (signal, col. 7 line 25 – col. 8 line 20), and to output (transferred, col. 7 lines 25-58) a signal representative of the identified input channel.

Referring to claim 19, Abe discloses a method of signal processing comprising connecting each of a plurality of input channels (Fig. 2 ref. signs 47-54 and respective portions of the spec.) in a predetermined repeating (repeat, col. 4 lines 50-58, col. 5 lines 35-40 and col. 8 lines 35-40) sequence to a common multiplexer output (Fig. 2, see the arrow going from the multiplexer to the A/D Converting Unit) via respective multiplexer inputs, and connecting the common multiplexer output to an output circuit (Fig. 2 ref. sign 45 and respective portions of the spec.), wherein the method further comprises detecting the presence at the common multiplexer output of a predetermined

signal (signal, col. 7 line 25 – col. 8 line 20), identifying the input channel which was the source of the detected predetermined signal (signal, col. 7 line 25 – col. 8 line 20), and outputting (transferred, col. 7 lines 25-58) a signal representative of the identified input channel.

9. Claims 1, 2 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kassatly (U.S. Patent No. 5,508,733).

Referring to claim 1, Kassatly discloses a signal processing apparatus (Fig. 1 and respective portions of the spec.) comprising a plurality of input channels (Fig. 1, Channel n , Channel 1 and Channel 2 and respective portions of the spec.) each of which is connected to a respective input of a multiplexer (Fig. 1 ref. sign 25 and respective portions of the spec.), the multiplexer being arranged to connect each input to a common multiplexer output (Fig. 1, To Receiver) in a predetermined repeating sequence (predetermined sequence, col. 59 lines 20-25), and an output circuit (Fig. 1 ref. sign 50 and respective portions of the spec.) connected to the common multiplexer output, wherein the output circuit is arranged to detect the presence at the common multiplexer output of a predetermined signal (signal, col. 19 line 25 – col. 20 line 46), to identify the input channel which was the source of the detected predetermined signal (signal, col. 19 line 25 – col. 20 line 46), and to output (transmitted, col. 19 line 25- col. 20 line 46) a signal representative of the identified input channel.

Referring to claim 2, Kassatly discloses a signal processing apparatus according to claim 1, wherein a predetermined signal is provided continuously to one input channel of the predetermined sequence (predetermined sequence, col. 59 lines 20-25),

such that the output circuit will output a signal representative of that input channel, referred to hereafter as the marker channel (marker channel, Figures 30, 34, 35 and 36 and respective portions of the spec.), each time that it is connected to the multiplexer.

Referring to claim 19, Kassatly discloses a method of signal processing comprising connecting each of a plurality of input channels (Fig. 1, Channel n , Channel 1 and Channel 2 and respective portions of the spec.) in a predetermined repeating sequence (predetermined sequence, col. 59 lines 20-25) to a common multiplexer output (Fig. 1, To Receiver) via respective multiplexer inputs, and connecting the common multiplexer output to an output circuit, wherein the method further comprises detecting the presence at the common multiplexer output of a predetermined signal (signal, col. 19 line 25 – col. 20 line 46), identifying the input channel which was the source of the detected predetermined signal (signal, col. 19 line 25 – col. 20 line 46), and outputting (transmitted, col. 19 line 25- col. 20 line 46) a signal representative of the identified input channel.

Allowable Subject Matter

10. Claims 6, 10, 14, 16, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. **Any response to this action should be mailed to:**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(571) 273-8300, (for formal communications intended for entry)

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamal A. Fox whose telephone number is (571) 272-3143. The examiner can normally be reached on Monday-Friday 6:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to 2600 Customer Service whose telephone number is (571) 272-2600.

Jamal A. Fox

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER